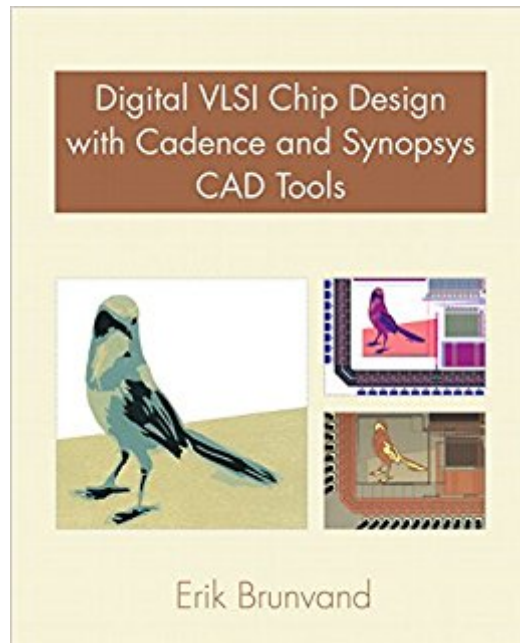




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Digital VLSI Chip Design With Cadence And Synopsys CAD Tools



Synopsis

KEY BENEFIT: This hands-on book leads readers through the complete process of building a ready-to-fabricate CMOS integrated circuit using popular commercial design software. **KEY TOPICS:** The VLSI CAD flow described in this book uses tools from two vendors: Cadence Design Systems, Inc. and Synopsys Inc. Detailed tutorials include step-by-step instructions and screen shots of tool windows and dialog boxes. **MARKET:** A useful reference for chip designers.

Book Information

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Customer Reviews

Digital VLSI Chip Design with Cadence and Synopsys CAD Tools leads students through the complete process of building a ready-to-fabricate CMOS integrated circuit using popular commercial design software. Detailed tutorials include step-by-step instructions and screen shots of tool windows and dialog boxes. This hands-on book is for use in conjunction with a primary textbook on digital VLSI. University instructors may order Digital VLSI Chip Design with Cadence and Synopsys CAD Tools with the following textbooks: [Rabaey Cover Image] Digital Integrated Circuits, 2nd Edition, by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikoli . To order Digital Integrated Circuits, 2nd Edition packaged with Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, please use ISBN 0-13-509470-4 on your bookstore order form. [Weste Cover Image] CMOS VLSI Design, 3rd Edition, by Neil H.E. Weste and David Harris. To order CMOS VLSI Design, 3rd Edition packaged with Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, please use ISBN 0-13-509469-0 on your bookstore order form. For further details, please contact your

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Professor Erik Brunvand is an associate professor in the School of Computing at the University of Utah. He has interests in computer architecture and VLSI systems in general, and self-timed and asynchronous systems in particular. One aspect of his research involves compiling concurrent communicating programs into asynchronous VLSI circuits. The current system allows programs written in a subset of occam, a concurrent message-passing programming language based on CSP, to be automatically compiled into a set of self-timed circuit modules suitable for manufacture as an integrated circuit. He is also interested in investigating the effects of asynchrony on computer systems architecture at a higher level. To explore these ideas he is building a series of prototype asynchronous computer systems out of FPGA and custom VLSI chips.

I wanted to implement a test chip with custom-design standard cell library elements. I wanted to take an RTL design and perform synthesis, backend (place and route), and top-level chip assembly (with other custom components) using a 0.13 um technology and an accompanying standard cell library. My background prior to reading this book was exclusively custom chip design, though I was familiar with HDL coding (for FPGAs). Going through this book allowed me to learn the digital ASIC design flow, and provided enough details for me to figure out how to incorporate my own custom-designed standard cells, which required some hacking and/or modifications to the standard design flow. As you read through this book, there will be plenty of areas of confusion, and the sample scripts will not work without modification to your specific design software setup. However, I gave the book five stars based on the relative value it provides over reading the user manuals of the software tools individually or searching the web. P.S. the test chip worked!

Fantastic text using insight, background material, and overall knowledge from premier user in EDA design tools. Erik does a tremendous job of explaining things and providing step by step detail in using complex VLSI design tools for creating design flows. I have known Erik for several years and he amazes me in his level of compassion, knowledge, and gift of teaching in a very complex area. This book is excellent for users both in the academic and commercial world who are looking for a guide that will help users learn the material well and provides a great reference for those that already have backgrounds in this area. This is a book that belongs on everyone's bookshelf not to mention having it very close by for reference while doing anything of importance in VLSI. More

importantly, Erik provides the files for users, so that they can follow along and create their own libraries.

I highly recommend this book for anyone who is setting up Cadence/Synopsys tool flow with the NCSU design kit. I have setup the complete flow (analog, digital, mixed-mode sims., and from laying out std. cells using the template, to synthesis and place and route -- including generating the necessary timing and abstract files) in Cadence using only this book and the scripts provided. ALL scripts can be found online at the book's website. Doing a simple web search of the author's name, UofU, or the book's title will point you to the book's webpage. You should keep in mind the purpose of this book is NOT to teach you about libraries, synthesis, place and route, and other VLSI topics. This book assumes you understand VLSI design flow and concepts. Again, I highly recommend this book for anyone who needs to set up the tool flow.

It is an ideal book for starter to learn the design flow of digital implementation using Cadence and Synopsys platform. The usages of the tools are described (much better than reading the long manuals). However, I think the starters usually cannot do the steps as smoothly as described in the book, since the users usually will encounter some error messages. The book seldom mention the method to solve the error messages displayed by the tools.

Digital VLSI Chip Design with ~~~ Book's Papers is not good. (likely newspaper's paper)

I have put my purchase on 11-Oct-2010. The expected arrival date is 20-oct-2010. Yet until now I still have not received my item.

This book addresses a very hard problem - teaching the essentials of designing VLSI digital circuits using the industrial-strength Cadence environment. As a longtime user of Cadence IC tools in the analog/RF design area, I am finding it to be very educational as I work to bring up the digital flow to support our increasingly complex mixed-signal designs. The book addresses exactly what I needed - navigating through the maze of software tools offered by Cadence. It does not cover IC process technology, nor the Verilog language - making the correct point that these are covered more than adequately elsewhere. What it does do is address the software tools, and it does so with well written text supported by many figures. This is exactly what I needed. I have no illusions everything will work exactly as described. Having struggled through learning Cadence tools on my own for years, I

understand the task the author has taken on is enormous. I am therefore willing to accept more struggles, but these will be much reduced thanks to the guidance I am finding in this book. Even if the NCSU toolkit or the UoU standard cells don't work for me, I don't care. I can learn from the book and use it guide me in the use of standard-cell based design in my favorite foundaries. I read 5 chapters on a recent airline trip, and was impressed enough with the knowledge gained that I bought 4 more copies to share with my graduate students. At the price offered by , I think this is a real bargain and will save my team hundreds if not thousands of dollars in personnel time!

This book provides a good introduction to synopsys and cadence software, however it is not without many flaws. First of all, throughout the book the author reference the University of Utah libraries which are supposed to be available online, but were nowhere to be found. This made it very difficult for me to follow along, since I was using the NCSU libraries which are claimed to be supported by this book, but are not fully. This book seems like it was written for a specific purpose (to teach U of U students how to use VLSI design software the way it is set up on their campus). That's great, but it doesn't belong in published book format. Also, when the author finally discusses synthesis using design compiler / vision, he does a terrible job explaining how libraries work and where to find them. Once again, it assumes you are using the set-up at U of Utah and its all there for you.

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